ABSTRACT OF THE DISCLOSURE

A semiconductor device test circuit that prevents unnecessary data from being inputted to a functional macro circuit at the time of testing the functional macro circuit. In a plurality of flip-flops connected in series, serial test pattern data latched by a flip-flop at a stage is latched by a flip-flop at the next stage in synchronization with a first clock signal. The test pattern data latched by flip-flops at all the stages is outputted to the functional macro circuit at once in synchronization with a second clock signal inputted to the flip-flops.